High Efficiency Single Synchronous Buck PWM Controller for INTEL VCCIN AUX ICL and TGL

General Description

The RT6543A/B PWM controller provides high efficiency, excellent transient response, and high DC output accuracy for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM.

The RT6543A/B supports on chip voltage programming function between 0V and 1.8V by controlling VID1/VID0 inputs.

Compared with conventional current-mode PWMs, the RT6543A/B achieves high efficiency without any current sensing resistors. Furthermore, the RT6543A/B has ability to drive synchronous rectifier MOSFETs and enters diode emulation mode at light load condition that also save lots of power consumption. Besides, the RT6543A/B equips with UVLO, OVP, UVP, OTP and current limit protection. All above functions are integrated in a WQFN-20L-3x3 package.

Applications

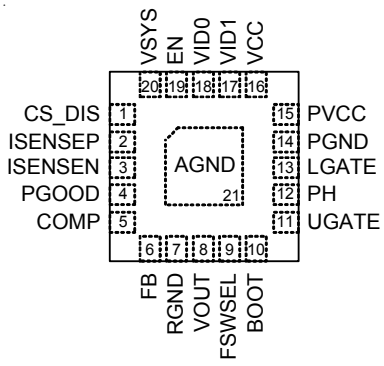
- Notebook Computers
- CPU/GPU Core Supply
- Chipset/RAM Supply
- Generic DC-DC Power Regulator

Features

- **A High Efficiency Step-Down DC-DC Controller**
- **Built-in 1% Reference Voltage**
- **2-Bit Programmable Output Voltage with Integrated**
- **Adjustable Switching Frequency**
- **Input Voltage Range : 3V to 24V**
- **Internal Soft-Start to Reduce Inrush Current**
- **Capability of Driving Large Synchronous Rectifier MOSFETs**
- **Power Good Indicator**
- **Cycle-by-Cycle Current Limit**
- **Over-/Under-Voltage Protection**
- **Thermal Shutdown**
- **RT6543A : Slew Down Mode as VID Change**
- **RT6543B : Decay Down Mode as VID Change**

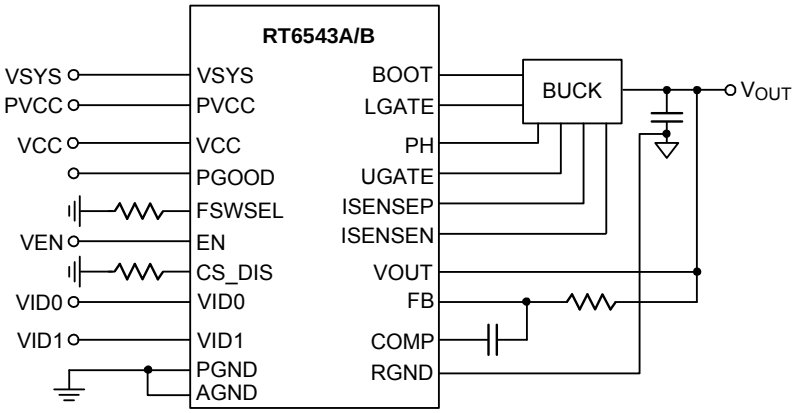
Pin Configuration

(TOP VIEW)



WQFN-20L 3x3

Simplified Application Circuit



Ordering Information

RT6543A/B □□

- Package Type
  QW : WQFN-20L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Mode when VID changes to lower set point
  A : Slew down
  B : Decay down

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

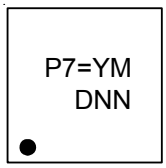
Marking Information

RT6543AGQW

ML= : Product Code

YMDNN : Date Code

RT6543BGQW



P7= : Product Code

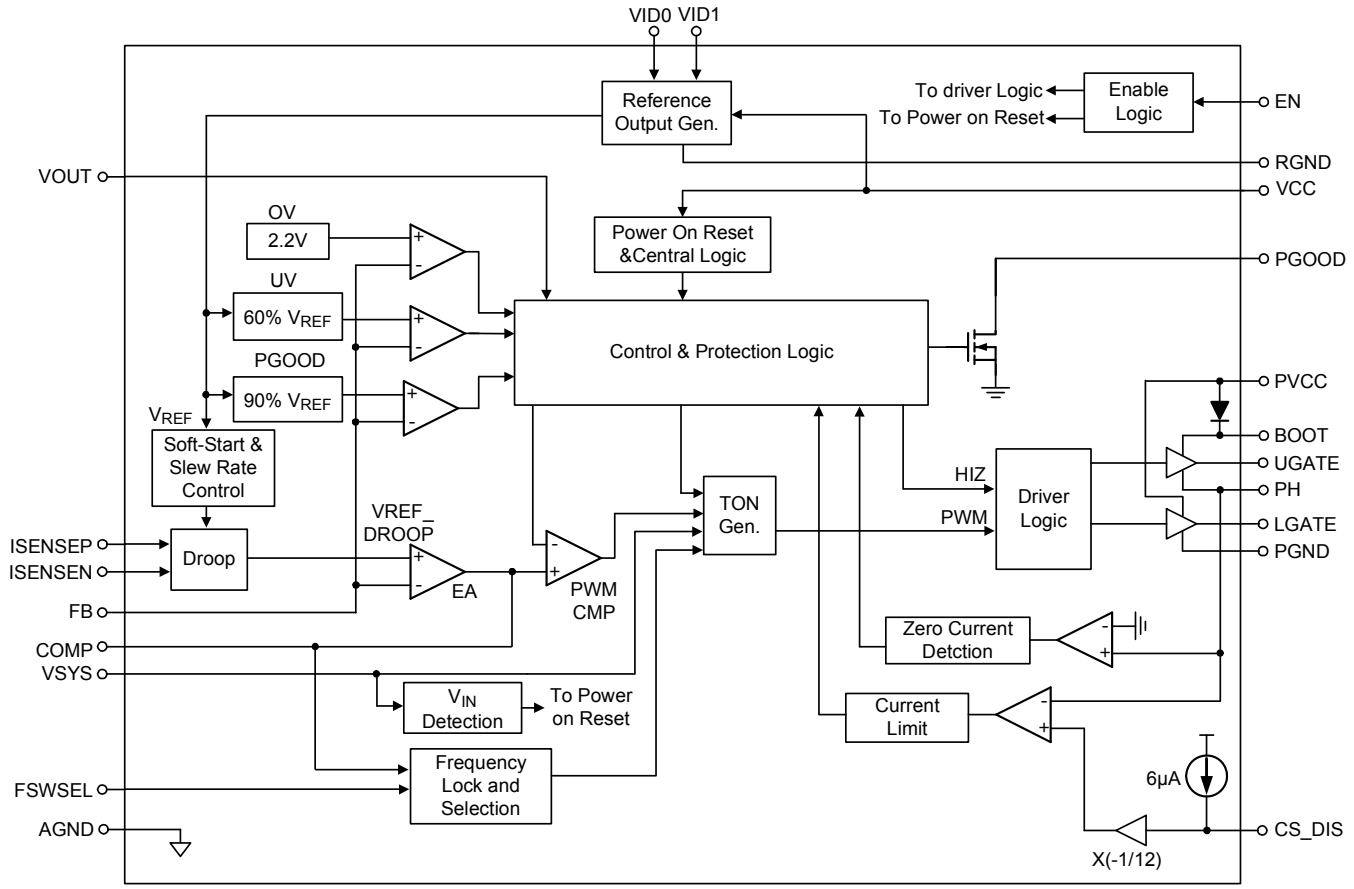
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	CS_DIS	Current limit setting. Connect a resistor from CS pin to AGND for overcurrent protection. CS pin sources a CS current which is 6μA (typ) at T_A = 25°C to define maximum allowable output current. CS terminal voltage VCS is limited from 0.5V to 2.8V over all operation temperature.
2	ISENSEP	Positive input pin for current sense of buck.(for load line setting, in zero load line condition is short this pin with ISENSEN)
3	ISENSEN	Negative input pin for current sense of buck.(for load line setting, in zero load line condition is short this pin with ISENSEP)
4	PGOOD	Power good indicator output for VCCIN_AUX. This open-drain is pulled low as UVP, OVP, OTP, EN low and output voltage is not regulated (such as before soft-start). An external pull-up resistor to VCC or other external rail is required, in which the pull-up resistor is recommended from 10kΩ to 100kΩ.
5	COMP	Internal error amplifier output. For loop compensator application.
6	FB	Internal error amplifier input. For loop compensator application.
7	RGND	Return ground for VCCIN_AUX from CPU side.
8	VOUT	VCCIN_AUX feedback input. This pin is unit feedback for AUX regulation
9	FSWSEL	VCCIN_AUX setting pin. Use this pin to adjust AUX rail frequency setting for different LC combination. (High state: Direct pull high to VCC, Hi-Z state: Floating, Low state: Direct connect to GND). Default switching frequency is floating, 600kHz. Anytime, make sure FSWSEL – VCC < 0.5V.
10	BOOT	Supply bootstrap capacitor output pin. The bootstrap capacitor is charged by this pin while the low-side MOSFET is turned on. Therefore, the bootstrap capacitor can provide the energy to turn on the high-side MOSFET. Connect this pin through the bootstrap capacitor to the PH pin.
11	UGATE	Upper gate driver with sink and source output. Connect to the gate of the high-side MOSFET through a short and low inductance path.
12	PH	Switch node of AUX. Connect to the power inductor. For the high-side gate driver return path, connect a capacitor from PH to BOOT. Beside, this pin is noisy, keep the sensitive trace or signal away from PH.

Pin No.	Pin Name	Pin Function
13	LGATE	Low-side gate driver output pin. Connect this pin to the gate of low-side MOSFET. Notice, DO NOT connect the resistor RG_EXT between LGATE and gate terminal of low-side MOSFET, otherwise it might cause undesired shoot-through since the LGATE voltage is monitored for shoot-through protection.
14	PGND	Power GND. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
15	PVCC	Bias voltage for internal gate driver. The required bias voltage for PVCC is 5V typ. For avoiding noise disturbance, the supplied bias voltage must be stable, Beside, a RC filter (R = 2.2Ω/0603 and C = 1μF/0603) from bias voltage to PVCC pin is necessary which should be placed as close as physically possible to PVCC pin.
16	VCC	Bias voltage for control logic. The required bias voltage for VCC is 5V typ. For avoiding noise disturbance, the supplied bias voltage must be stable, Beside, a RC filter (R = 2.2Ω/0603 and C = 1μF/0603) from bias voltage to VCC pin is necessary which should be placed as close as physically possible to VCC pin.
17	VID1	VCCIN_AUX VID control signal. Adjust AUX output voltage (0V, 1.1V, 1.65V and 1.8V)
18	VID0	VCCIN_AUX VID control signal. Adjust AUX output voltage (0V, 1.1V, 1.65V and 1.8V)
19	EN	Enable control input. As voltage is lower than 0.3V, RT6543A/B is in shutdown mode and all power rails are disabled. As RT6543A/B is higher than 1V, RT6543A/B is woken up.
20	VSYS	System voltage sense. Connect this pin to input voltage for UVLO monitor and controller's on-time setting. For avoiding any noise to disturb on-time setting, a RC filter (R = 2.2Ω/0603 and C = 0.1μF/0603) is required from input voltage to VSYS.
21 (Exposed pad)	GND	Exposed pad for package. Electrically isolated. Directly solder to the large PGND plane and use thermal vias to connect PGND of other layers for thermal resistor reduction

Functional Block Diagram



Operation

The RT6543A/B is a constant on-time synchronous step-down controller. In normal operation, the high-side N-MOSFET is turned on when the output voltage is lower than V_{REF}, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Soft-Start (SS)

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

PGOOD

The power good output is an open-drain architecture. When the soft-start is finished, the PGOOD open-drain output will be high impedance.

Current Limit

The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The current limit threshold can be set with an external voltage setting resistor on the CS_DIS pin.

Over-Voltage Protection (OVP) & Under-Voltage Protection (UVP)

The output voltage is continuously monitored for over-voltage and under-voltage protection. When the output voltage exceeds 2.2V (Typ.), UGATE goes low and LGATE is forced high. When the feedback voltage is less than 60% of output voltage, under-voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until VCC is re-supplied and exceeds the POR rising threshold voltage or EN is reset.

Absolute Maximum Ratings (Note 1)

- VSYS to PGND ---------- –0.3V to 28V
- VCC to PGND ---------- –0.3V to 6.5V
- RGND to PGND ---------- –0.3V to 0.3V
- BOOT to PH ---------- –0.3V to 6.5V
  - DC ---------- –0.3V to 6.5V
  - <100ns ---------- –2V to 7.5V
- BOOT to PGND
  - DC ---------- –0.3V to 30V
  - <100ns ---------- –10V to 35V
- LGATE to PGND
  - DC ---------- –0.3V to 6.8V
  - <100ns ---------- –2V to 7.5V
- PH to PGND
  - DC ---------- –0.3V to 30V
  - <100ns ---------- –10V to 35V
- UGATE to PGND
  - DC ---------- –0.3V to 36.8V
  - <100ns ---------- –10V to 41.8V
- Other Pins ---------- –0.3V to 6.8V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-20L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  - WQFN-20L 3x3, θ_{JA} ---------- 30°C/W
  - WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VCC Input Voltage ---------- 4.5V to 5.5V
- VSYS Input Voltage ---------- 3V to 24V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, V_{SYS} = 7.4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage VCC						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{SHDN}	V_{EN} = 0V	--	5	--	μA
	I_{DACOFF}	V_{EN} = 5V, VID = 00	--	40	--	μA
	I_{VCC}	V_{EN} = 5V, no switching	--	0.3	0.55	mA
VCC POR/UVLO Threshold						
POR Threshold	V_{CC_POR}		4	4.2	4.4	V
UVLO Threshold	V_{VCC_UVLO}		3.7	3.9	4.1	V
Logic Threshold						
VID0/VID1 Input Low Voltage	V_{ID_IL}	Falling edge, V_{CC} = 5V	--	--	0.3	V
VID0/VID1 Input High Voltage	V_{ID_IH}	Rising edge, V_{CC} = 5V	1	--	--	V
EN Input Low Voltage	V_{EN_IL}	Falling edge, V_{CC} = 5V	--	--	0.3	V
EN Input High Voltage	V_{EN_IH}	Rising edge, V_{CC} = 5V	1	--	--	V
FSWSEL Input High Level	V_{FSWSEL_H}	Rising edge, V_{CC} = 5V	4.5	--	--	V
FSWSEL Input Low Level	V_{FSWSEL_L}	Falling edge, V_{CC} = 5V	--	--	0.4	V
FSWSEL Input Floating Level	V_{FSWSEL_HIZ}	Floating, V_{CC} = 5V	2	2.5	3	V
VSYS UVLO						
VSYS UVLO Threshold	V_{SYS_UVLO}		--	2.7	--	V
UVLO Hysteresis	V_{SYS_HYS}		--	200	--	mV
Input Current	I_{VSYS}	V_{SYS} = 19V, V_{CC} = 5V	--	2	--	μA
		V_{SYS} = 8.4V, V_{CC} = 5V	--	0.9	--	μA
		V_{CC} < V_{CC_UVLO}	--	0	--	μA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Indicator (upper side threshold decide by OV threshold)						
PGOOD High Threshold	V_{PGOOD_IH}	Rising edge	86	90	94	$\%V_{OUT}$
PGOOD Low Threshold	V_{PGOOD_IL}	Falling edge	80	84	88	$\%V_{OUT}$
PGOOD Leakage Current	I_{LK_PGOOD}	High state, V_{PGOOD} = 5V	--	--	1	μA
PGOOD Output Low Voltage	V_{PGOOD_LOW}	I_{PGOOD_LOW} = 10mA	--	--	0.3	V
Input Supply Voltage						
Supply Voltage	V_{IN}		3	--	24	V
Reference and Soft-Start						
Output Voltage Scaling		VID[1:0] = 11	1.782	1.8	1.818	V
		VID[1:0] = 10	1.6335	1.65	1.666	
		VID[1:0] = 01	1.089	1.1	1.111	
		VID[1:0] = 00	–0.01	0	0.01	
Dynamic Voltage Scale Slew Rate	SR_{DVS}		12	--	40	mV/μs
Current Limit						
Current Limit	I_{LIM}		5.4	6	6.6	μA
Current Limit Setting Range	V_{CS}	Voltage of pin CS_DIS	0.4	--	2.8	V
Current Limit Voltage	$V_{\_PHASW\_OC}$	GND – PHASE = VCS / 12 0.5V ≤ VCS ≤ 2.8V	–15	VCS / 12	+15	%
		GND – PHASE = VCS / 12 0.4V ≤ VCS ≤ 0.5V	–7	VCS / 12	+7	mV
Current Limit Temperature Coefficient			--	4700	--	ppm/°C
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}	FSWSEL = 5V	--	0.8	--	MHz
		FSWSEL = HIZ	--	0.6	--	
		FSWSEL = 0V	--	0.4	--	
Switching Frequency Programmable Step			--	200	--	KHz
Switching Frequency Accuracy	f_{SW}	FSWSEL = HIZ	0.51	0.6	0.69	MHz
Minimum Off-Time	t_{OFF_MIN}		--	130	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protections						
OVP Trip Threshold	V_{OVP}	OVP detect	2.05	2.2	2.35	V
OVP Deglitch Time	t_{DGL_OVP}		--	5	--	μs
UVP Trip Threshold	V_{UVP}	UVP detect	48	60	72	%
UVP Deglitch Time	t_{DGL_UVP}		--	5	--	μs
Zero Current Crossing Threshold	V_{PH_ZC}		–4	--	4	mV
Driver						
UGATE Driver Source	$R_{UGATEsr}$	BOOT – LX = 5V	--	2	4	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOT – LX = 5V	--	1	2	Ω
LGATE Driver Source	$R_{LGATEsr}$	LGATE, high state, V_{CC} = 5V	--	1.5	3	Ω
LGATE Driver Sink	$R_{LGATEsk}$	LGATE, low state, V_{CC} = 5V	--	0.7	3	Ω
Dead Time	t_{D_LU}	From LGATE falling to UGATE rising	--	30	--	ns
	t_{D_UL}	From UGATE falling to LGATE rising	--	20	--	ns
Internal Boost Diode Resistance	R_{BOOT}	VCC to BOOT, I_{BOOT} = 10mA	--	40	80	Ω
Discharge Resistance						
Discharge Resistance	R_{DISCHG}	AUX	--	50	--	Ω

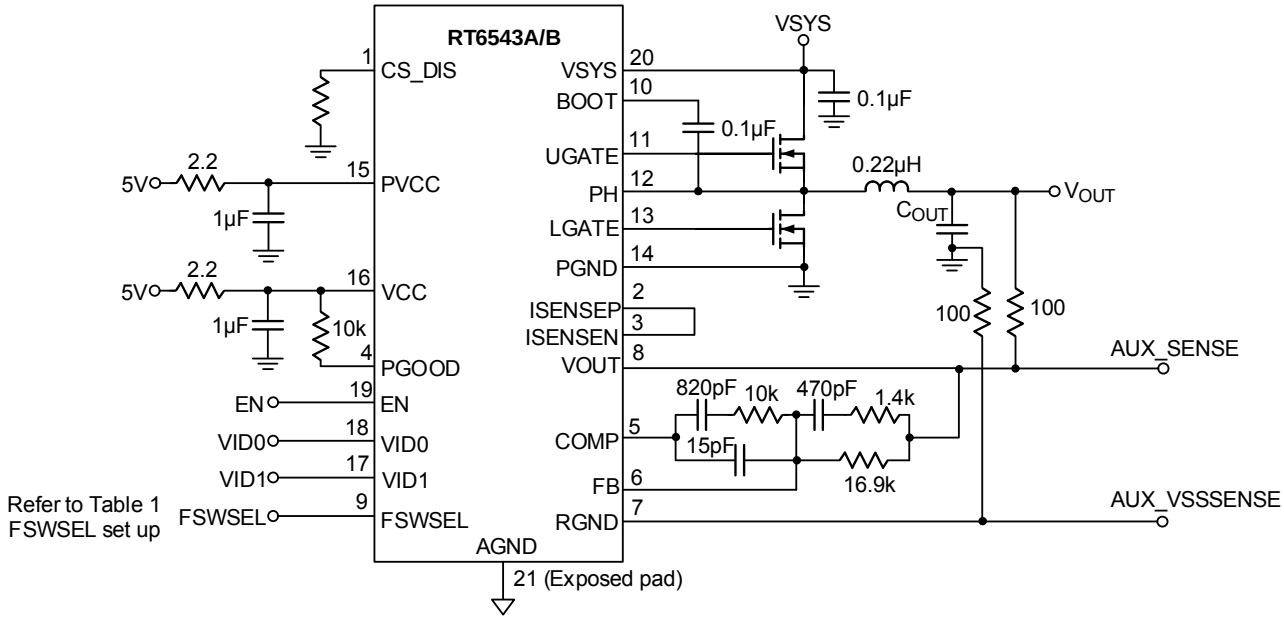
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



C_{OUT}	Y-Line (PCS)	U-Line (PCS)
ICL	17	22
TGL	19	20

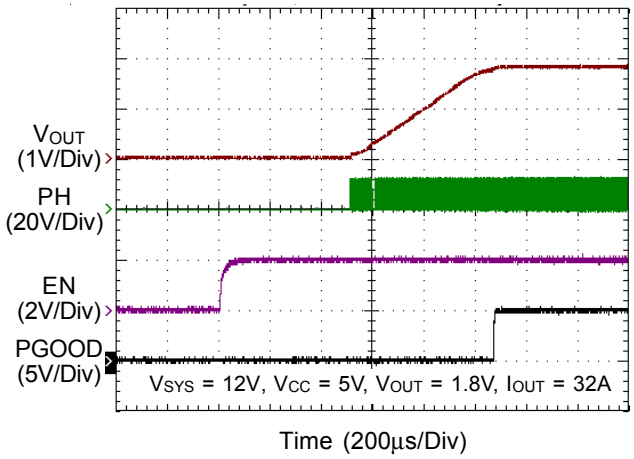
C_{OUT} type : 22µF/6.3V

Table 1. FSWSEL set up

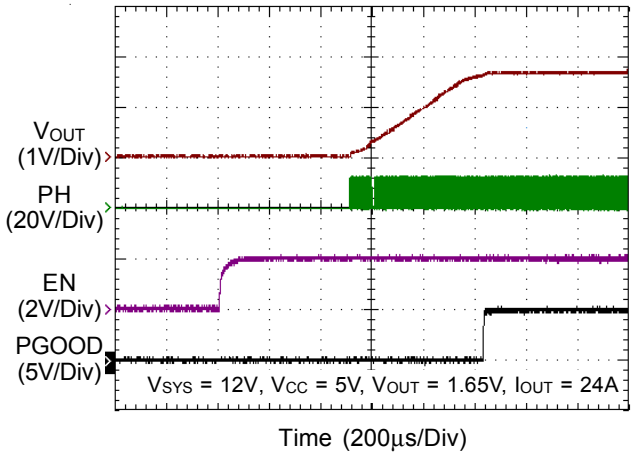
FSWSEL	Frequency setting	Suggestion
High (>4.5V)	800kHz	Connect to VCC
Floating (2~3V)	600kHz	Floating
Low (<0.4V)	400kHz	Connect to GND

Typical Operating Characteristics

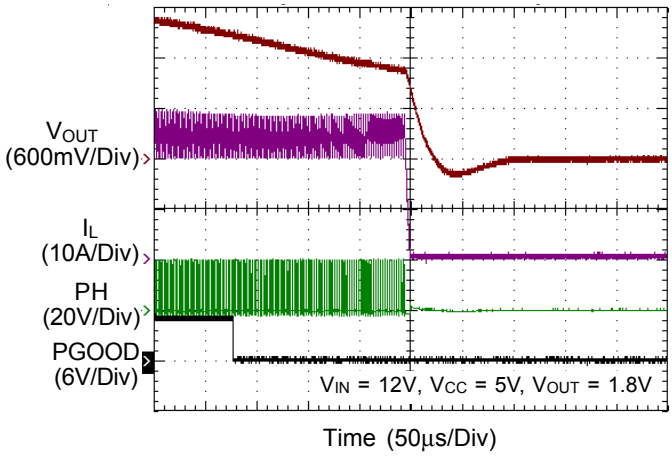
Power On from EN



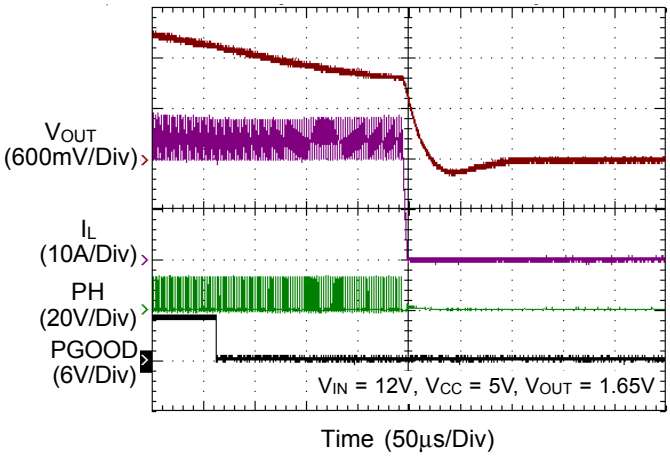
Power On from EN



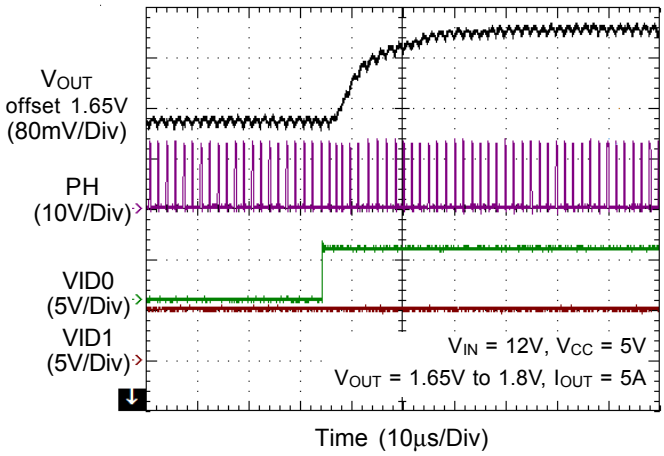
Over-Current Limit



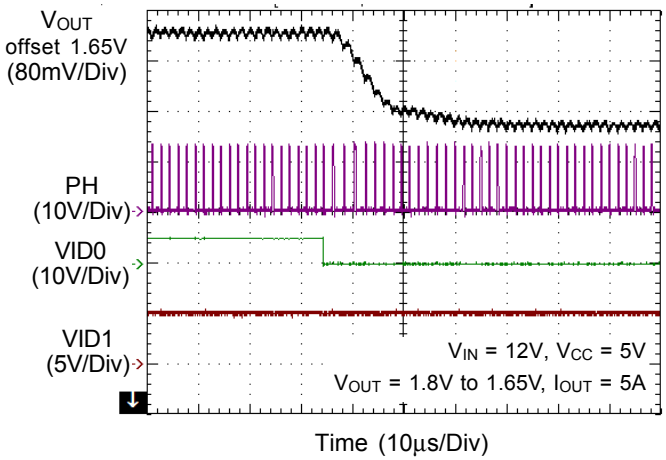
Over-Current Limit



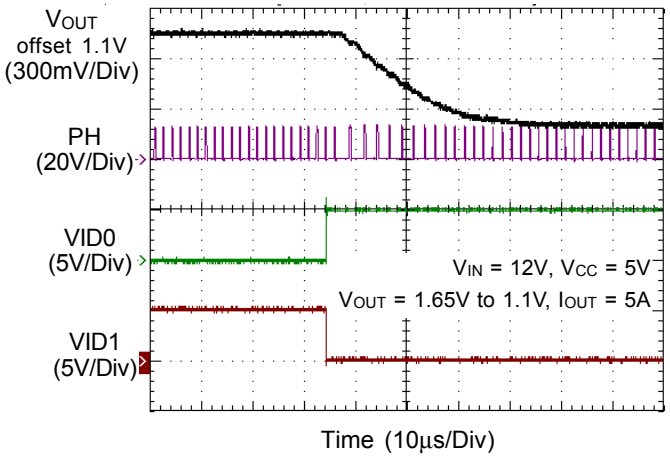
VID Change



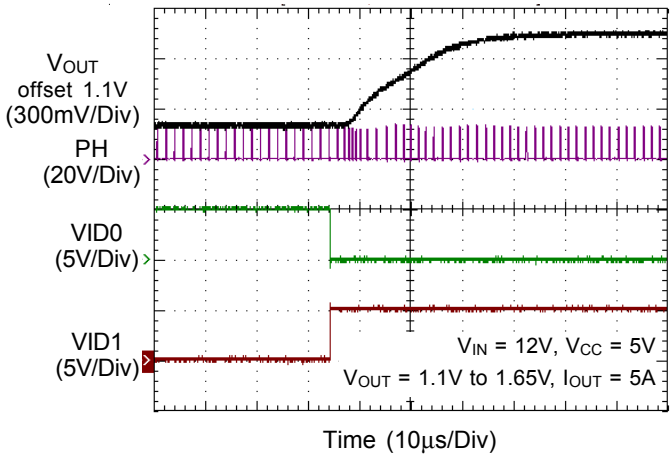
VID Change



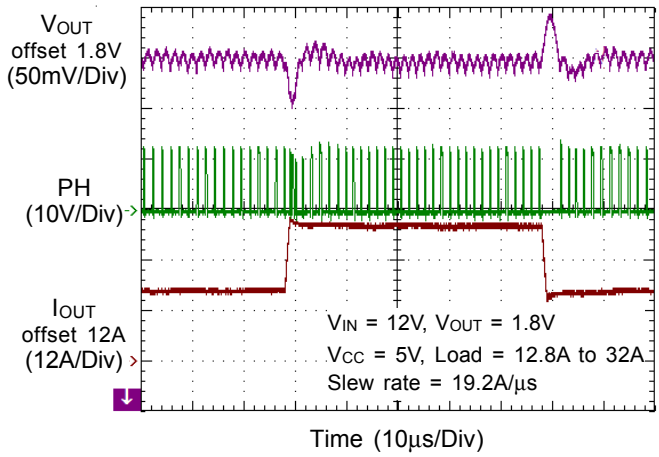
VID Change



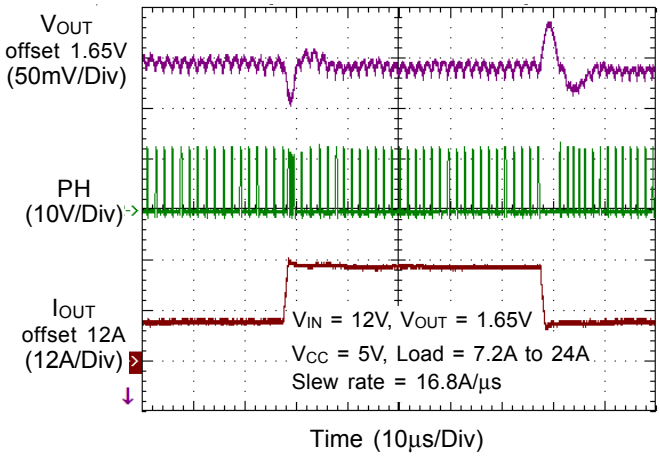
VID Change



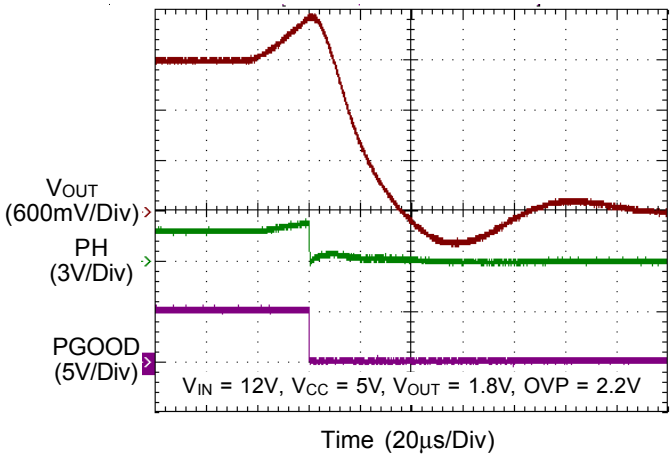
Load Transient Response



Load Transient Response



Over-Voltage Protection



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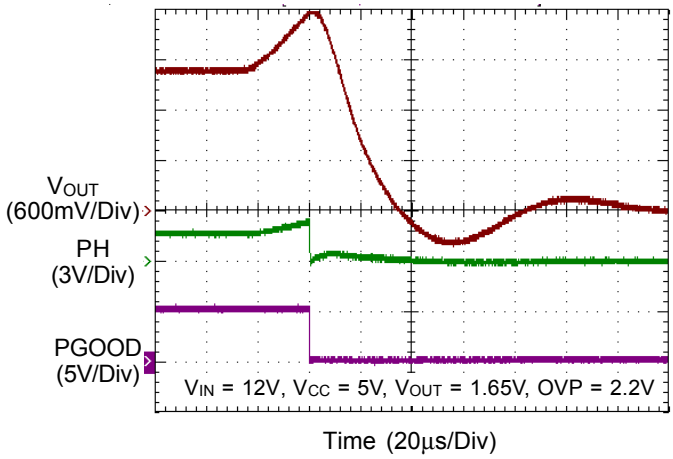
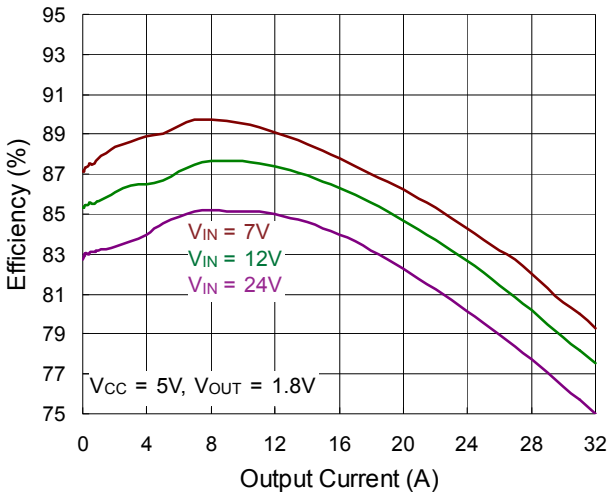
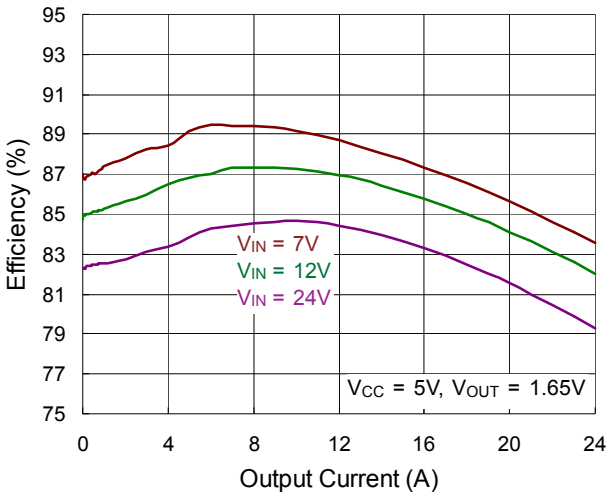


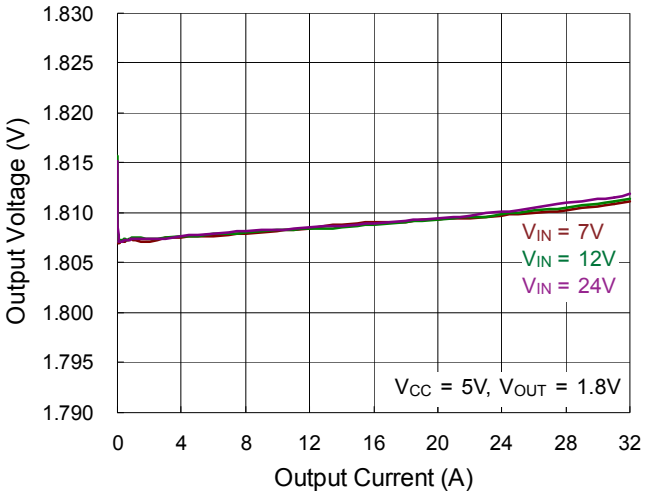
V1P8 Efficiency vs. Output Current



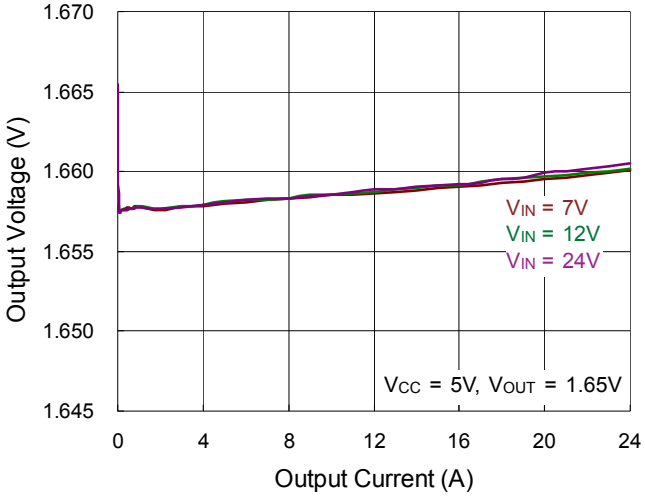
V1P65 Efficiency vs. Output Current



Output Voltage vs. Output Current



Output Voltage vs. Output Current



Application Information

The RT6543A/B is a constant on-time PWM controller which supports on chip voltage programming function (0V, 1.1V, 1.65V and 1.8V) by controlling VID1/VID0 inputs. The control scheme uses in the RT6543A/B is called FCOT™ (Fixed Constant On-Time) which easy handles wide input/output ratios and provides fast response to load steps while maintains a relatively constant operating frequency.

FCOT™ is provided a solution to solve a problem of poor load transient timing in current mode PWM, and performs excellent noise immunity for suiting comprehensive applications.

PWM Operation

FCOT™ control scheme relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. Referring to the function block diagrams of the RT6543A/B, the synchronous high-side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the high-side MOSFET is turned off. The pulse width of this one-shot is determined by the converter's input and output voltages for keeping the frequency fairly constant with entire input voltage range. Besides, the pulse width of low-side one-shot is set as 130ns(typ.) minimum off-time.

On-Time Control (t_{ON})

There are two inputs on on-time one-shot comparator. One input is used to detect input voltage and then transfer to proportional current. The transferred current is applied to charge to on-time capacitor till threshold V_{OUT} connected to the other input of comparator. Further, the on-time is determined, relating to V_{IN} and V_{OUT}. This implementation results in a nearly constant switching frequency without any clock generators.

Diode Emulation Mode (DEM)

In diode emulation mode, the RT6543A/B automatically reduces switching frequency at light load conditions to maintain high efficiency. Therefore, during period of discontinuous conduction mode, for emulating the behavior of diode, the few negative current is allowed to flow through the low-side MOSFET when inductor's free-wheeling current is in negative status. On the other hand, as the load current increasing from light load to heavy load, the switching frequency raises to the expected value where inductor current is in continuous conduction mode. Figure 1 shows the behavior of inductor current in boundary conduction mode and the load current can be expressed as below :

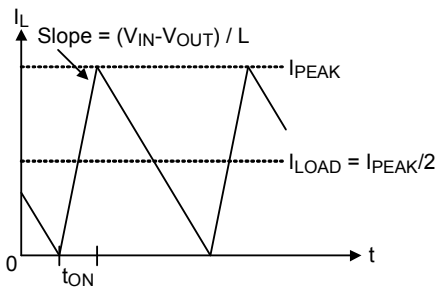


Figure 1. Boundary Condition of CCM/DEM

$$I_{LOAD(SKIP)} = \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

Output Voltage Transition Operation

Through controlling the digital pins VID0 and VID1, V_{OUT} can be changed to setting output voltage. During the downward transition (V_{OUT} from high to low condition), internal V_{REF} is adjusted to a new V_{REF} by converting VIDx signal. During this period, the low-side MOSFET is turned on to pull down the output voltage V_{OUT}. LGATE is remained high until V_{FB} falls to the new internal V_{REF} and UGATE goes high to start a new cycle, as shown in Figure 2.

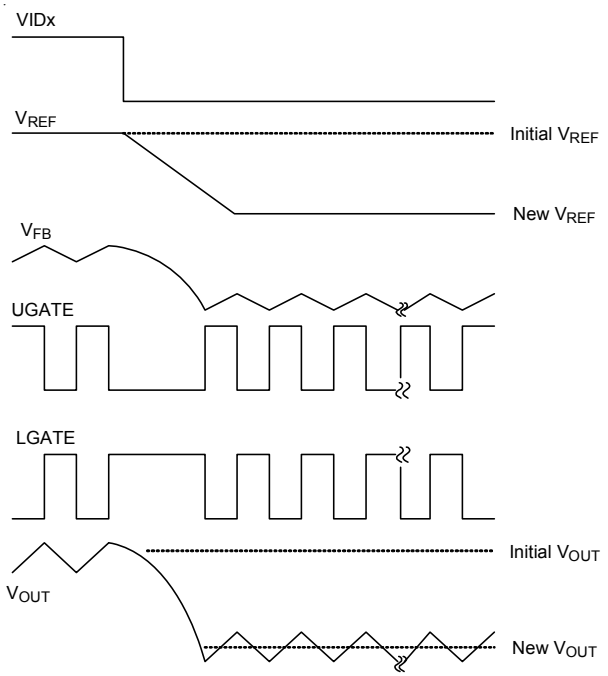


Figure 2. Down Transition of Output Voltage

During the upward transition (V_{OUT} from low to high), internal V_{REF} is raised to the new level V_{REF} through VIDx change. At this moment, V_{FB} is increased to new V_{REF}. However, for handling fast transition of output voltage, the switching frequency is speeded up and the minimum off-time is limited as 130ns (typ.) till V_{FB} is over the new V_{REF}.

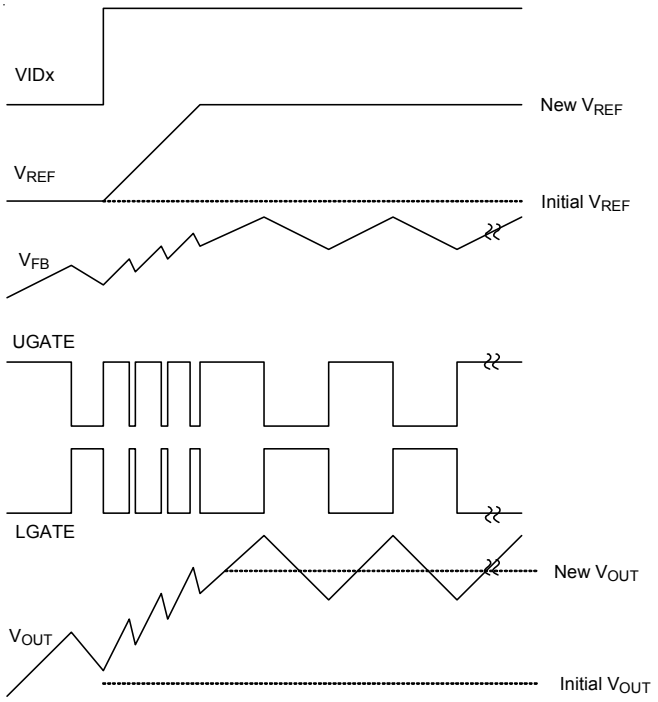


Figure 3. Upward Transition of Output Voltage

If the V_{OUT} change is too significant, UGATE continues to output several cycle with minimum off-time. At the same time, inductor current is rapidly increase which leads to storage energy LI^2 of inductor flowing to output capacitor after V_{FB} achieving new V_{REF}. This causes an enormous overshoot on V_{OUT}, as shown in Figure 4.

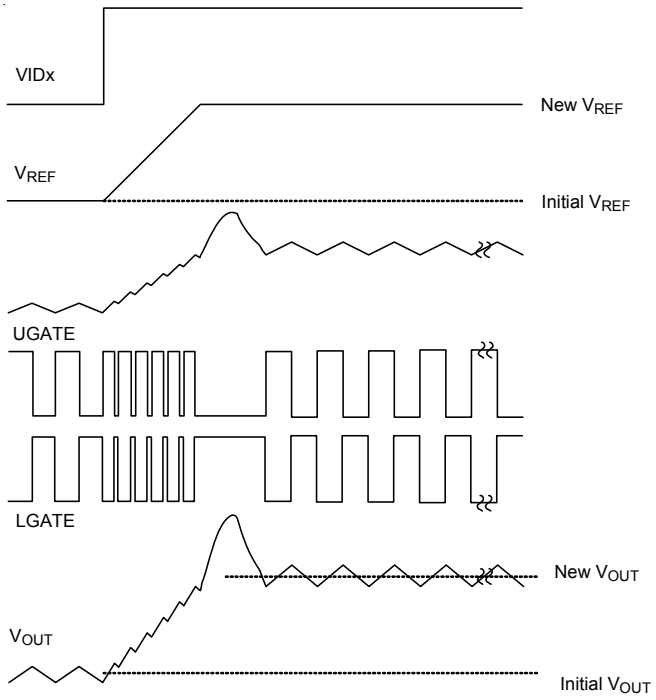


Figure 4. Overshoot of Output Voltage During Upward Transition

The overshoot voltage can be approximately calculated in following expression, where I_{CL} is the current limit level and V_{FINAL} is the desired set point of final V_{OUT}.

$$V_{MAX} = \sqrt{\frac{I_{CL}^2 \times L}{C_{OUT}} + V_{FINAL}^2}$$

Droop Setting and Thermal Compensation

The RT6543A/B provide droop setting via DCR network as Figure 5. Due to the cooper wire of inductor has a positive temperature coefficient.

And hence, temperature compensation is necessary for the lossless inductor current sense. For thermal compensation, an NTC Thermistor is put in the current sense network and it can be used to compensation DCR variation from temperature is changed.

The DCR network equation is as follows :

$$V_{ISENSEP-ISENSEN} = I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \times \frac{1 + \frac{L}{DCR}s}{1 + \frac{R_X \times R_{EQ} \times C}{R_X + R_{EQ}}s}$$

$$\text{Let } R_{EQ} = R_S + \frac{R_P \times R_{NTC}}{R_P + R_{NTC}}$$

According to current sense network, the corresponding equation is represented as follows :

$$\frac{L}{DCR} = \frac{R_X \times R_{EQ} \times C}{R_X + R_{EQ}},$$

$$\text{then } V_{ISENSEP-ISENSEN} = I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}}$$

If DCR network time constant matches inductor time constant, L/DCR, an expected load transient waveform can be designed.

The droop set equation as follows :

$$V_{DROOP} = \left(I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}}\right) \times 8$$

$$R_{DCLL} = \frac{V_{DROOP}}{I_L} = DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \times 8$$

Where, 8 is internal parameter of RT6543A/B.

For detail DCR network calculation, Richtek provide design for customer in order to simplify design.

$$\text{Note : } \left(I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}}\right) \text{must be < 25mV}$$

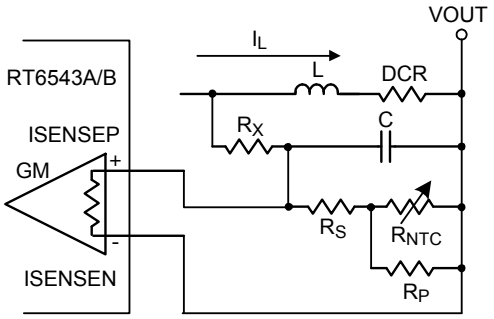


Figure 5. DCR Sense Circuit and Thermal Compensation

Current Limit Setting

The RT6543A/B provides a cycle-by-cycle current limiting function that is implemented by a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at the CS_DIS pin is above the current limit threshold, the PWM is not allowed to initiate a new cycle as shown in Figure 6. In order to provide both good accuracy and a cost effective solution, the RT6543A/B supports temperature compensation for MOSFET $R_{DS(ON)}$ sensing.

The CS_DIS pin is connected to GND through a trip voltage setting resistor R_{CS}. The RT6543A/B sources a 6μA current I_{CS} to R_{CS}, and current limit level V_{CS} can be defined as follows :

$$V_{CS} = R_{CS} \times 6\mu A$$

The inductor valley current detection is completed by monitor low-side MOSFET voltage during period of UGATE in low status. Hence, the relationship between current limit level V_{CS} and over current setting point I_{OCP} can be defined as follows :

$$I_{OCP} = \frac{V_{CS}}{12 \times R_{DS(ON)\_LS}} + \frac{I_{L\_ripple}}{2}$$

$$= \frac{V_{CS}}{12 \times R_{DS(ON)\_LS}} + \frac{1}{2 \times L \times f_{sw}} \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN}}$$

As over current condition is triggered, the duty cycle is limited, and, further, V_{OUT} starts to drop. If V_{OUT} drops to under-voltage protection level, the RT6543A/B is into latch mode. Only EN or V_{CC} being reset, the RT6543A/B can be released from latch mode.

Note that the VCS should be set from 0.4V to 2.8V.

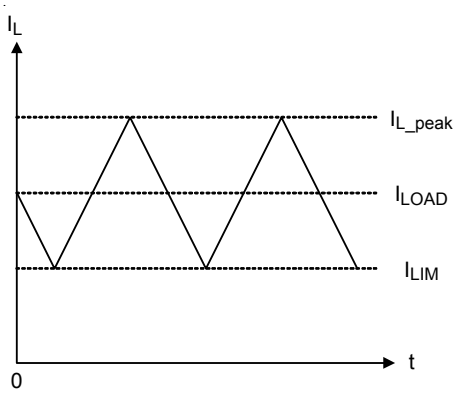


Figure 6. "Valley" Current Limit

MOSFET Gate Driver (UGATE, LGATE)

The high-side driver is designed to drive high current and low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, 5V bias voltage is delivered from V_{CC}. The average driving current is proportional to the gate charge at V_{GS} = 5V and is supplied from a flying capacitor connected between BOOT and PH pins. On the other hand, the low-side driver is used to drive high current and low $R_{DS(ON)}$ N-MOSFET, which is relied on V_{CC} supplies 5V bias voltage. Due to the instantaneous driving current sourced from V_{CC}, V_{CC} must connect a fly capacitor to GND. Besides, for

preventing short through occurrence within the region of high and low-side MOSFETs transition, there is a dead time between UGATE and LGATE.

Power Good Output (PGOOD)

The power good output is an open drain output that requires a pull-up resistor. As output voltage is lower than 16% (typ.) setting voltage, PGOOD will be pulled low. In other words, if output voltage is higher than 90% (typ.) setting voltage, PGOOD will be pulled high. In soft-start period, PGOOD is held low till soft-start function is over and output voltage reaches 90% setting voltage.

POR, UVLO and Soft-Start

Power On Reset (POR) occurs when VCC rises above 4.2V (typ). After POR is triggered, the RT6543A/B resets the fault latch and starts a new operation cycle. If V_{CC} is below 3.9V, the RT6543A/B is into under-voltage lockout (UVLO), which is forced UGATE and LGATE in low status. Furthermore, the RT6543A/B provides an internal soft-start function for preventing great inrush current and output overshoot during converter turn-on period. After EN is enable, the RT6543A/B operating in soft-start period, ramp of internal reference voltage is clamped to compare with FB signal that, further, limits converter's turn-on time.

Output Over-Voltage Protection and Under-Voltage Protection

For preventing output voltage raising above regulation level to damage next stage components, the RT6543A/B provides output over-voltage protection (OVP). If output voltage is over OVP level, UGATE remains low status. At the same time, LGATE is pulled high till the inductor current reaches zero or next on-time one-shot is triggered. As output voltage upon OVP threshold lasts over 5μs (typical), OVP function is triggered.. In addition, the RT6543A/B also supplies output under-voltage protection (UVP). If output voltage below UVP threshold continues over 5μs (typical), UVP function is triggered. Both of protection functions are behaved latch-off mode in the RT6543A/B. Once the protection is triggered, the RT6543A/B goes to shut-down and stops switch. Only toggle EN or re-power on V_{CC}, the RT6543A/B can relief protection situation and work.

Over-Temperature Protection

The RT6543A/B includes an over-temperature protection (OTP) circuitry to prevent overheating caused by excessive power dissipation. As junction temperature is over 160°C, OTP circuitry will be triggered and then shuts down the RT6543A/B into latch mode. Only toggle EN or re-power on V_{CC} again, the RT6543A/B can relief protection situation and restart.

For continuous operation and adequate cooling, the junction temperature does not exceed 160°C.

External Bootstrap Capacitor (C_{BOOT})

Connect a 0.1μF low ESR ceramic capacitor between BOOT pin and PH pin. This bootstrap capacitor provides energy to drive high-side N-channel MOSFET. If high-side MOSFET is turned too fast to pass EMI, a small resistor (<10Ω) can be added between BOOT and the external bootstrap capacitor. This move will slow high-side MOSFET turn-on and then improve EMI ability.

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductance benefits from reduced size and cost and improves the circuit's transient response. However, lower inductance also leads to greater inductor ripple current and output ripple voltage, while efficiency is reduced. Conversely, higher inductance might gains more efficiency, but inductor's size and resistance will be physically larger because of more turns of wire required. As well, higher inductance slows transient response, because inductor needs more time to achieve volt-second balance.

For designing a good compromise between size, efficiency and transient response, inductor ripple current (ΔI_L) is considered which is specified from 20% to 50% of the desired full output load current. Calculate the approximate inductance by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating the percentage current of $I_{OUT(MAX)}$ with ΔI_L.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductance is chosen, the ripple current (ΔI_L) can be calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, saturation current rating and thermal rating of selected inductor must exceed $I_{L(PEAK)}$, where are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may design current rating up to the current limit value. However, the IC's output under-voltage shutdown feature makes this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements.

Input Capacitor Selection

High quality ceramic capacitor, such as X5R or X7R, with values greater than 20μF are recommended for input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material behaves less capacitance variation and more temperature stability. Voltage and current rating are the key parameters to select an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated by using following equation :

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{IN}}{C_{IN} \times f_{SW} \times V_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The typical operating circuit is recommended to use four 10μF and low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT6543A/B are optimized for ceramic output capacitors and best performance. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple is made up of output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and have to be considered.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. FCOT™ transient response is very quick and output transients are usually small. The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is related to load step, output capacitor value, inductor value, input-to-output voltage differential, and the maximum duty cycle. Hence, the approximate on-time (neglecting parasitic) and maximum duty cycle can be calculated from given input and output voltages, as follows :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

According to calculated D_{MAX}, the output sag voltage can be obtain. As follows :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is related to the load step, the output capacitor value, the inductor value and the output voltage. Therefore, output soar voltage can be determined, as below :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for a WQFN-20L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

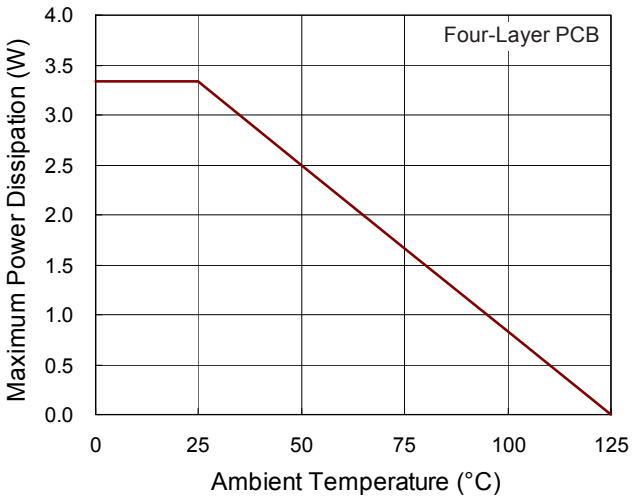


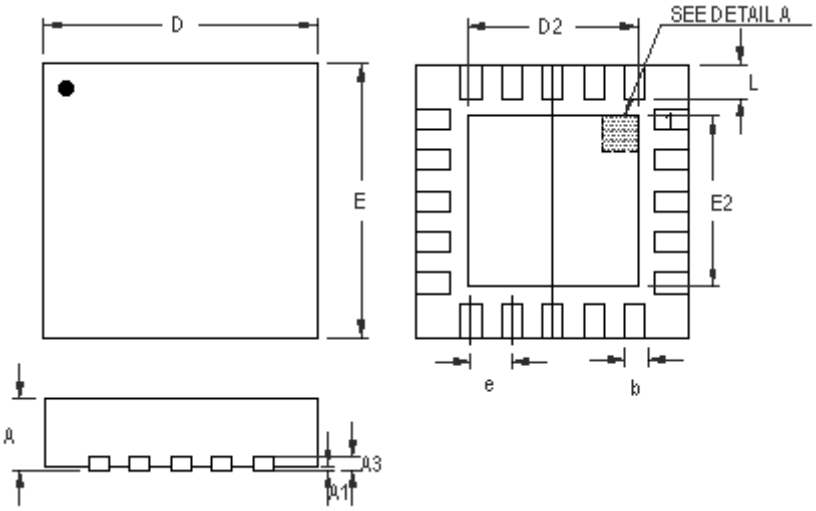
Figure 7. Derating Curve of Maximum Power Dissipation

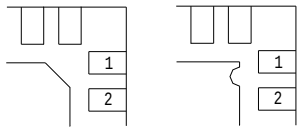
Layout Considerations

Layout is very important in high frequency switching converter design. If the design is improper, the PCB could radiate excessive noise and contribute instability in converter. For the best performance of the RT6543A/B, the following guidelines should be strictly followed.

- Connect a RC low-pass filter from V_{CC}, (1μF and 10 are recommended). Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should be kept away from high voltage switching nodes to prevent it from coupling.
- Connecting between the drivers and the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- All the sensitive analog traces and components, such as FB, GND, EN, PGOOD, CS and VCC, should be placed away from high voltage switching nodes (PHASE, LGATE, UGATE, or BOOT) nodes to prevent coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made by Kelvin connections to ensure an accurate signal.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Outline Dimension





DETAIL A

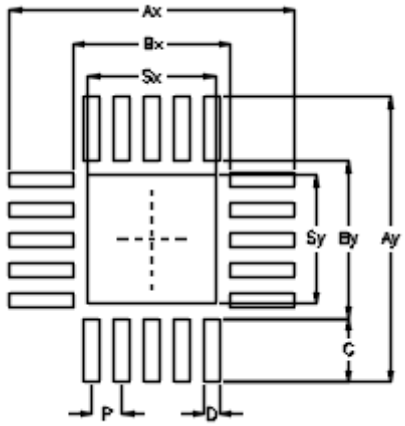
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-20	20	0.40	3.80	3.80	2.10	2.10	0.85	0.20	1.70	1.70	±0.05

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